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**Code No: A6508**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M.Tech I Semester Examinations, March/April-2011**
**LOW POWER VLSI DESIGN**
**(WIRELESS AND MOBILE COMMUNICATION)**

**Time: 3hours** **Max. Marks: 60**

**Answer any five questions**
**All questions carry equal marks**

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1. a) Explain about the scaling limitation for low voltage, low power design. Give the effect of scaling on various MOSFET parameters with necessary equations.
   b) Explain about the various drain structures used in BICMOS process integration. [12]

2. a) What is drain induced barrier lowering. Explain how it gets effected in short channel MOSFETS.
   b) Explain about the shallow trench isolation technique. [12]

3. a) Compare the conventional BICMOS process flow and PRET.
   b) Distinguish between various BSIM models of FET. [12]

4. a) Explain the various driver configurations in the BICMOS logic circuit family.
   b) Explain the operation of a bootstrapped type BICMOS digital circuit. [12]

5. a) Explain the intrinsic Gummel-poon model.
   b) Draw the CMOS implementation of 2 input XOR gate. [12]

6. a) Explain about the model parameters extraction for developing an analytical model.
   b) Explain about the space charge current model. [12]

7. a) What is the need for low power latches and flip flops. Also explain the uses of latches and flip flops.
   b) Explain the setup time and hold time consideration in flip flops? [12]

8. Write short notes on any **two**
   a) Silicon on Insulator
   b) ESD free BiCMOS
   c) Chemical mechanical polishing. [12]

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